		Application/Control No.	Applicant(s)/Patent Under Reexamination
Notice of References Cited		09/757,373	USSERY ET AL.
		Examiner	Art Unit	
		Phallaka Kik	2825	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2002/0133784	09-2002	Gupta et al.	716/1
	B	US-6,477,697	11-2002	Killian et al.	716/18
	C	US-6,665,862	12-2003	Isman, Marshall A.	717/127
	D	US-6,047,115	04-2000	Mohan et al.	716/16
	E	US-6,167,559	12-2000	Furtek et al.	716/16
	F	US-6,701,431	03-2004	Subramanian et al.	713/1
	G	US-6,519,753	02-2003	Ang et al.	716/16
	H	US-6,421,817	07-2002	Mohan et al.	716/16
	I	US-6,216,257	04-2001	Agrawal et al.	716/16
	J	US-5,737,235	04-1998	Kean et al.	716/16
	K	US-6,408,428	06-2002	Schlansker et al.	716/17
	L	US-6,701,515	03-2004	Wilson et al.	717/117
	M	US-6,163,836	12-2000	Dowling, Eric M.	712/37

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	WO 9959078 A1	11-1999	World Intellect	BRIGHTMAN et al.	G06F 15/16
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Iseli et al., "Spyder: a reconfigurable VLIW processor using FPGAs", 1993 Proceedings of IEEE Workshop on FPGA for Custo Computing Machines, 5 April 1993, pp. 17-24.
	V	Schuette et al., "Exploiting instruction-level resource parallelism for transparent, integrated control-flow monitoring", Twenty-Fir International Symposium on Fault-Tolerant Computing, 25 June 1991, pp. 318-325.
	W	Bombana et al., "IP-based design of custom field programmable network processors", 1998 IEEE International Conference on Electronics, Circuits and Systems, Vol. 1, 7 September 1998, pp. 467-471.
	X	Wazlowski et al., "PRISM-II compiler and architecture", 1993 Proceedings of IEEE Workshop on FPGAs for Custom Computing Machines, 5 April 1993, pp. 9-16.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-2002/0010853	01-2002	Trimberger et al.	713/1
	B	US-6,408,382	06-2002	Pechanek et al.	712/227
	C	US-5,956,518	09-1999	DeHon et al.	712/15
	D	US-5,896,521	04-1999	Shackleford et al.	703/21
	E	US-6,360,259	03-2002	Bradley, Peter C.	709/223
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Kneip et al., "Parallel implementation of medium level algorithms on a monolithic ASIMD multiprocessor", 1996 IEEE International Symposium on Circuits and Systems, Vol. 4, 12 May 1996, pp. 316-319.
	V	NN86112519, "Dynamically Reconfigurable Microprocessing System", Vol. 29, No. 6, November 1986, pp. 2519-2523 (6 pages
	W	Chien et al., "MORPH: a system architecture for robust high performance using customization (an NSF 100 TerOps point desig study)", Sixth Symposium on the Frontiers of Massively Parallel Computing, 27 October 1996, pp. 336-345.
	X	Kidwell et al., "Automatic synthesis of parallel proc ssors", 1991 IEEE International Symposium on Circuits and Systems, Vol. 11 June 1991, pp. 3158-3161.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.